



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Blandy**

Serial No.: **09/671,875**

Filed: **September 28, 2000**

For: **Apparatus and Method for  
Creating Instruction Bundles in an  
Explicitly Parallel Architecture**

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Group Art Unit: **2183**

Examiner: **Tsai, Henry**

Attorney Docket No.: **AUS9-2000-0587-US1**

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. 1.97

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

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**APR 02 2004**  
**Technology Center 2100**

Applicants request that the information listed on the attached Form PTO-1449 be considered by the Office during the pendency of the above entitled application, pursuant to 37 C.F.R. 1.97.

Please charge any fees necessary for prosecution of the present application to Deposit Account No. 09-0447. If any extension of time is required, such extension is hereby requested. Please charge any additional required fee for extension of time to Deposit Account No. 50-0392.

In accordance with 37 C.F.R. 1.97(h), the filing of this Information Disclosure Statement shall not constitute an admission that any information cited therein is, or is considered to be, material to patentability as defined in 37 C.F.R. 1.56(b). In the interest of full and complete disclosure to the Office, some or all of the art cited herein may not be considered by Applicant(s) or the Undersigned to be material under the new standards of materiality defined in 37 C.F.R. 1.56(b), enacted March 16, 1992, but may be material under the old standard of materiality defined in 37 C.F.R. 1.56(a), last amended on November 28, 1988, or may merely be technical background which

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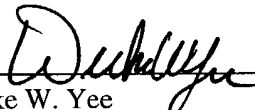
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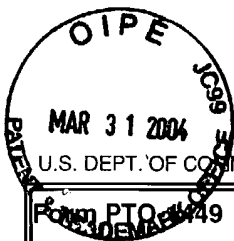
may be of interest to the Examiner. In accordance with 37 C.F.R. 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made.

This Information Disclosure Statement is being filed before the mailing date of a final action or a notice of allowance. A check for the required fee of \$180.00 as set forth in § 1.17(p) is enclosed.

Respectfully submitted,

Date: 3/29/04

  
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<b>LIST OF PRIOR ART CITED BY APPLICANT</b> <i>(Use several sheets if necessary)</i>	ATTORNEY DOCKET NO. <b>AUS9-2000-0587-US1</b>	SERIAL NO. <b>09/671,875</b> <div style="text-align: center; font-weight: bold; font-size: 1.2em;">RECEIVED</div> <div style="text-align: center; font-weight: bold;">APR 02 2004</div>
APPLICANT <b>Blandy</b>		<div style="text-align: right; font-weight: bold;">Technology Center 2100</div>
FILING DATE <b>September 28, 2000</b>		GROUP ART UNIT <b>2183</b>

**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL	DOCUMENT NO.	PUBLICATION DATE	INVENTOR NAME	CLASS/ SUBCLASS	FILING DATE
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	AB 6,539,473 B1	Mar. 25, 2003	Hubacher et al.	713/2	Sep. 2, 1999
	AC 6,487,601 B1	Nov. 26, 2002	Hubacher et al.	709/229	Sep. 30, 1999
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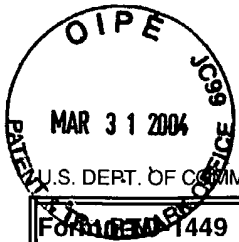
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	FILING DATE <b>September 28, 2000</b>	<b>Technology Center 2100</b>

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CH	Sinclair et al., "ASIC Design for Conditional Nested Loops with Predicate Registers", 08/11/1999, Circuits and Systems, 1999, 42 <sup>nd</sup> Midwest Symposium, vol. 2, pgs. 874-877.
CI	"The Java Virtual Machine Specification", Sun Microsystems, Inc., copyright 1997, <a href="http://java.sun.com/docs/books/vmspec/html/Instructions2.doc14.html">http://java.sun.com/docs/books/vmspec/html/Instructions2.doc14.html</a> .
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CK	Ishizaki et al., "Design, Implementation, and Evaluation of Optimizations in a Just-In-Time Compiler, ACM, 6/1999, pp. 119-122.

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